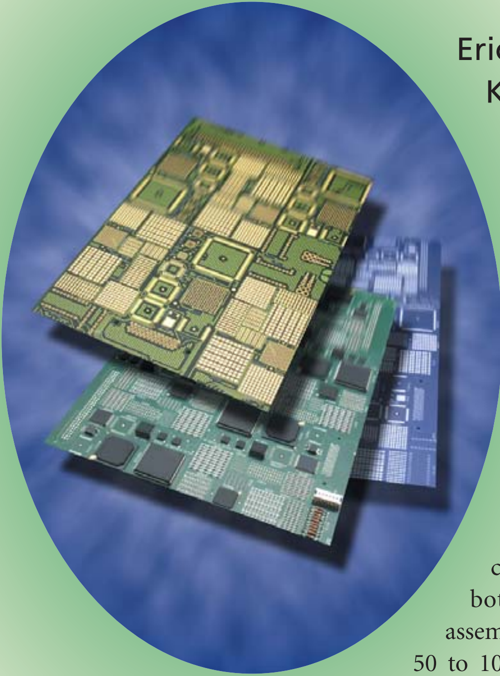
Reducing Solder Voids with Copper-Filled Microvias



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A study seeks to find out the frequency, location and size of voids with and without copper-filled vias.

Utilizing microvias in surface-mount pads on printed wiring boards (PWBs) has created unique challenges for both PWB fabricators and assemblers. Microvia structures of 50 to 100 microns are manufactured daily in high-volume production of ceramic chip carriers. In PWB fabrication, microvia structures are typically greater than 150 microns and utilize epoxy and polyimide-based substrates. These material sets require glass to limit z-axis expansion and, while providing cost savings, mandate stronger and more consistent copper deposits and solder joints.

Implementation of microvia-in-pad technology into PWB designs allows for tighter spacing of ball grid arrays (BGAs) and stacked via build-up techniques to eliminate less reliable plated through holes.[1] A small market exists today for organic integrated circuit (IC) substrates utilizing this type of build-up technology. This market segment has embraced the via-on-pad design concept and promoted the development of new plating technology used in metallization of the microvia.[2] These unique acid copper plating systems fill the microvia with copper while depositing nominal copper thickness on the PWB surface.

A microvia filled with copper eliminates many PWB fabrication and assembly problems. Fabrication of microvias has traditionally seen issues with entrapped corrosive process chemistry and continuity of the final finish.[3] By at least partially filling the microvias, wetting and rinsing during final PWB fabrication are not issues. The final result is overall improvement in long-term reliability. On the assembly side, a microvia in a surface-mount pad will be tented with solder paste during the printing process. This tenting causes a gas pocket to form in the microvia that expands into the solder joint during the reflow process (Figure 1a). The result is a large void in the solder joint.

Based on x-ray imaging, the IPC-7095 standard[4] specifies three categories for void size for BGA solder joints. These categories are based on the percentage of joint cross-sectional area occupied by the void:

- Class III, Small—void area is less than 9%
- Class II, Medium—void area is greater than 9%, but less than 20.25%
- Class I, Large—void area is greater than 20.25%, but less than 36%.

This standard does not specify a category for voids greater than 36%, assuming this figure is beyond acceptable limits of most products. Class III product is for highest reliability with the smallest allowable void area.

Void size is one aspect known to affect solder joint reliability. However, data demonstrating the influence of via filling on solder voids and solder joint reliability could not be found. As a first step, a study was undertaken to quantify the frequency, location and size of voids with and without copper-filled vias.

Solder Void Study Parameters[5]

The test vehicle was an eight-layer PWB with three different BGA designs ranging from 100 to 300 I/O at 1 mm pitch. Each PWB had five replicates of each BGA design, and all microvias were 100-micron diameter and 60 micron deep. The pad size for each BGA pad was 250 microns in diameter. The high-density interconnect (HDI) layer was made using 1080 prepreg with foil copper. With the glass present the resultant via structure had severe glass exposure and was less than optimum for plating performance (Figure 2). The glass protruding into the microvia made wetting of the microvia and copper plating more difficult. The final finish on all test vehicles was organic solderability protectant (OSP).

Eight test vehicles were plated in each of three acid copper processes. The control process provided conformal plating of the microvia. A standard-type acid copper formulation with high sulfuric acid and low copper metal was used.

The two developmental systems designated red and blue were high copper and low sulfuric formulas. Each used unique additives to provide various degrees of via filling.

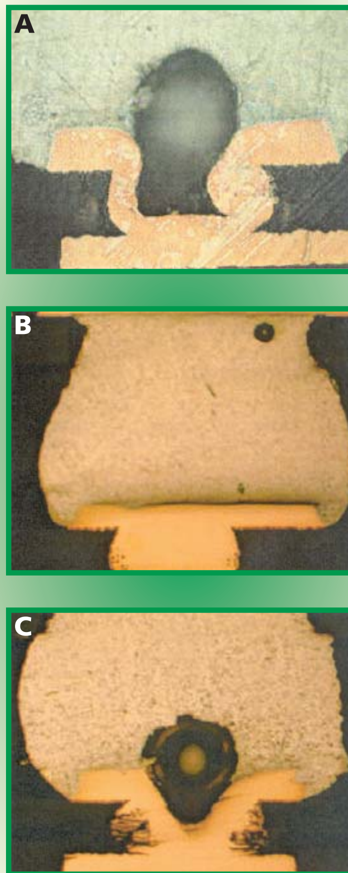

FIGURE 1: Acid copper processes: A) no fill; B) red process; C) blue process.

The red system gave the best via filling performance (Figure 1b). This process utilized a pre-dip to suppress the surface plating followed by a separate grain refiner system in the plating bath. The blue formulation is a newer development where the suppressor and grain refinement is all done in the plating process. In this test, the blue process gave less via filling than the red (Figure 1c). Under more optimum via geometries, via filling of the blue process is superior.

Cross sections were utilized to show void location, occurrence of voids and via filling success. X-ray data were collected, and x-ray analysis was used to measure void size and occurrence.

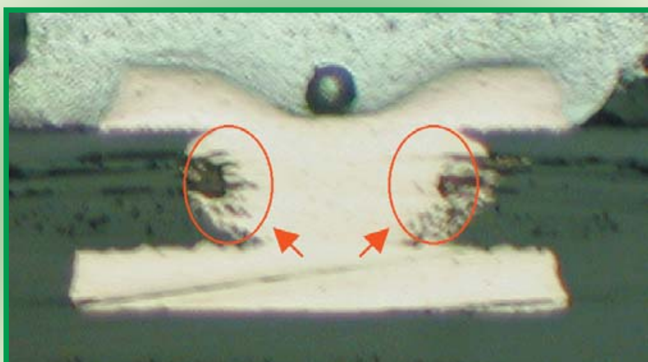

FIGURE 2: Poor via structure: protruding glass.

Several factors outside of via filling, such as reflow profile and paste chemistry, affect void occurrence in solder joints. To account for these parameters, four paste scenarios were included in this study:

- Control—Paste 1 with low voiding reflow profile
- Case 1—Paste 2, with supplier's recommended reflow profile
- Case 2—Paste 3 with straight ramp reflow profile
- Case 3—Paste 3 with low voiding reflow profile.

Specific paste chemistries were chosen to provide minimal to maximum amounts of volatile materials. Reflow parameters were set to allow maximum and minimum time for volatiles to escape. In this manner, a range of solder voiding was created to measure the true effect of via filling.

Solder Void Study Results

When evaluating voids in solder joints, different types of measurements need to be considered. The primary concern is typically void size or percentage of the solder joint area. As stated earlier, IPC 7095 standard allows different void sizes. However, the frequency of pads with voids and where the void occurs in the solder joint are thought to also influence solder joint reliability. Though reliability testing will be done at a later date, all three void measurements, size, frequency and location were done in this study.

Void size, as shown in Table 1, demonstrates filling vias with copper to be highly effective in reducing average void size. The average void size was 7.6% without via fill, 2.8% with partial fill and 2.0% with full via fill. Therefore, even partial filling from the blue process will dramatically reduce void size. More important, however, is the distribution of void size. Thirty-five percent of the voiding with no via filling is larger than Class III (larger than 9% in area), and 3% falls within the worst class, Class I. Class I is a reject for most products; when the vias are not filled, nine pads on a 300 I/O BGA will have a reject condition. With full via filling, 99% of the voids are within Class III, or smaller than 9% by area.

	Control Copper Process	Blue Copper Process	Red Copper Process
Sample Size (# of joints)	1940	1940	1940
Average Void Area (%)	7.6%	2.8%	2.0%
	Distribution of Void Size Per IPC-7095		
% Voids Class I	3%	0%	0%
% Voids Class II	32%	5%	1%
% Voids Class III	65%	95%	99%

TABLE 1: Average void size and distribution of void size.

The number of pads with solder voids or frequency of void occurrence was measured by both cross section and x-ray. Raw x-ray data and cross-section data did not agree on frequency of void occurrence. Cross-section data shown in Figure 3 indicates that non-filled vias have voids on 76% of the pads, partial filling (blue) reduces it to 39% and full via filling (red) reduces occurrence to 23%.

However, in this study x-ray data showed a high frequency of void occurrence (84 to 99%) for all three copper processes. The consistently high void occurrence is due to the high sensitivity of the x-ray system. X-ray analysis will detect voids or artifacts, such as solder surface dimples and copper plating voids, that are 2 to 3 microns in size or larger. However, a significant cutoff limit below which a void would be considered insignificant does not exist. The x-ray data agree with cross-section analysis if a minimum significant void size of 2.2% is used. To further base line x-ray data, additional work will be done on flat copper pads under each of the paste conditions outlined in this study.

Cross sections were used to evaluate the void location. The percent of voids near the PWB surface for each fill condition is shown in Figure 3. The voids, though larger with the unfilled (control) and partial filled (blue) vias (Figure 1), stay close to the PWB. In comparison, only 20% of smaller voids with total filled vias (red) stay near the PWB. Therefore, a pad with successful via fill has a mostly flat surface, while a pad with no via fill still has a cavity that can serve as an attachment point for a void. The effect of the location of small solder voids on reliability has not been tested at this time.

To monitor process consistency, solder paste print height was measured for all experimental conditions. An unexpected experimental variation in solder paste volume deposited for each condition was discovered. Solder paste deposits were significantly lower for the blue via filled boards. The three acid copper processes had different color solder mask to ensure easy identification of each test condition. The blue copper process yielded a copper deposit equal in height to the blue solder mask, which gave better stencil gasketing and less paste push through versus either the control or red process. Further analysis will be necessary to investigate the impact of solder paste volume on this study's results.

Conclusion

The purpose of this study was to determine the effect of via filling on void formation in solder joints. The study compared conformal copper plating to partial and full via filling with copper. Different solder paste chemistries and reflow profiles were selected to provide a range of potential solder voids. Both cross section and x-ray analysis were performed to measure void size, occurrence and location.

The data generated in this study demonstrate the benefits of filling vias with copper.

- Solder void size compared to conformal plating was reduced by 74% with full via fill.
- Partial filling produced almost equivalent results with 64% reduced solder void size.

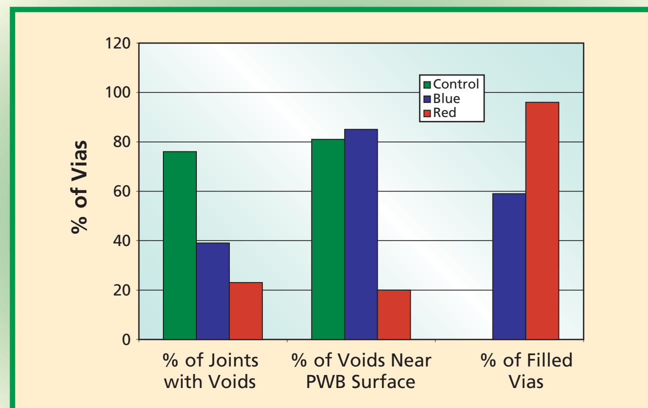

FIGURE 3: Void summary from cross-section data.

- Occurrence of voiding dropped from 76% to 39% and 23%, respectively, for partial and full via filling.

Solder joint voids were observed in the solder joint, not at the PWB surface, when the microvias were completely filled. How this result affects the reliability of the solder joint is unknown and will be part of future studies. In addition, baseline studies on solder void classification versus flat copper surfaces and solder paste volume are currently under way. Looking to the future, lead-free assembly, due to melting points, will only complicate assembly to via-in-pad and may require implementation of via fill to reduce solder voiding to an acceptable level.

Unique copper plating chemistries are being developed to fill microvias void free with copper. Microvias filled in this manner reduce solder void size and occurrence in microvia-in-pad designs. These new chemistries will allow the next generation product with via-in-pad and stacked via geometries to be built without major equipment investment for either PWB fabrication or assembly.

References

1. M. Ahmad, S. Teng, M. Hu, M. Brillhart, "Assessing the Reliability of Plated Vias," *PC FAB*, November 2002, pp. 30-37.
2. Prismark Partners LLC, September 2002.
3. D. Pauls, T. Munson, "Sulfates in Vias: The Rest of the Story," *Circuits Assembly*, March 1999, p. 94.
4. IPC-7095, August 2000.
5. A. Singer, P. Chouta, J. McLenaghan, "Internal Technical report 0163-TR002: Via-Fill for Microvia-in-Pad Void reduction," December 2002.

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