Imbedded Component/Die Technology

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Increased reliability—coupled with reduced size and weight—has demanded the evolution of assembly technology.

The U.S. Navy's Program Executive Office (PEO) Integrated Warfare Systems (IWS) 3A has authorized and funded a research and development contract for Soldering Technology International's (STI) patent-pending manufacturing technology, Imbedded Component/Die Technology (IC/DT). The technology for designing and manufacturing three-dimensional (3-D) circuit card assemblies (CCAs) addresses barriers in CCA design and fabrication, as well as the limitations in two-dimensional (2-D) printed circuit board (PCB) assembly.

The drive to chip-scale packages and multichip modules (MCMs) has made real estate a premium on 2-D substrates. The push to smaller form and fit factors has driven the component industry down the size curve from 1208s to 0804/0603s and ultimately 0201/0101s. A smaller form and fit factor is paramount in gaining real estate for higher input/output (I/O) applications.

IC/DT is a concept for eliminating secondary packaging and thermal management limitations. The technology uses the smallest form and fit factor components and die available with no secondary packaging. The imbedded technology places these components and bare die inside a PCB substrate in 3-D using the smallest amount of real estate required to meet the I/O objective (Figure 1).

The technique uses the smallest surface-mount devices (SMDs) and bare die available in their non–packaged state. PCB layout in 3-D allows designers to convert the electrical schematic's I/Os to the smallest form factor. Size reductions of 80% can be achieved by eliminating the secondary packaging of most components.

IC/DT Characteristics and Features

IC/DT eliminates unnecessary failure opportunities and uses reliable electrical interconnects. All external component packaging and solder joints are eliminated. Bare die are imbedded into an organic, laminate substrate and attached to a rigid, cooling core. Flexible electrical interconnects provide a reliable means of connecting I/O. Additional environmental protectants are used to protect the internal components from the environment.

Improved Reliability

The elimination of external component packaging improves overall CCA reliability by improving signal integrity, reducing electrical failure opportunities and reducing mass. Reducing the number of interconnects from an integrated circuit's output to the circuit eliminates failure opportunities.

Figure 2 shows a ball grid array (BGA) with three additional conductors that could result in points of failure, including wire bonds from the IC die to an interposer, traces on the interposer to the vias and then the solder spheres underneath the interposer, and finally the solder interconnect between the spheres and substrate bond pad. The elimination of component-level packaging also removes parasitic transmission line parameters from the component to the PCB. Parasitic resistance, inductance and capacitance are added with each conductor used to interconnect the signal to the PCB. Increased parasitics result in attenuation of signals and crosstalk.

Decreased Volumes of Material

The elimination of secondary packaging material creates mass savings (Table 1). Since the IC/DT design creates a protected environment to use components in bare die form, the external packaging of the component is no longer required. A reduction in the mass related to the attachment material

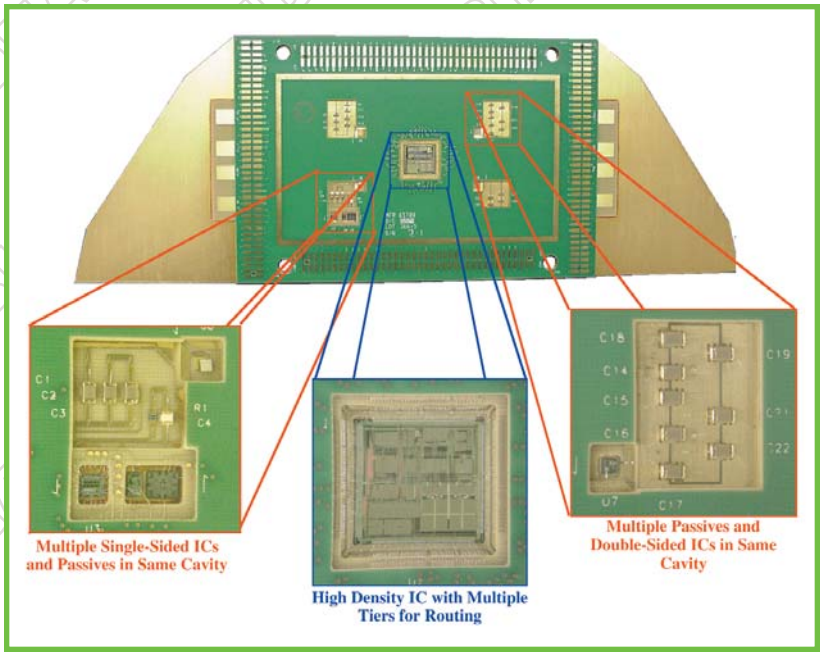

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FIGURE 1: IC/DT advantages and features.

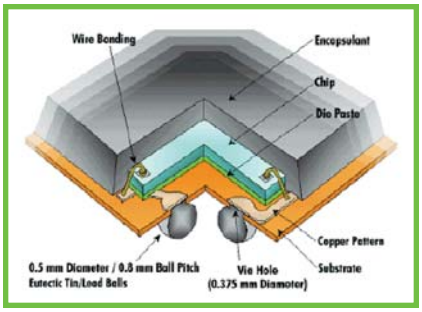

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FIGURE 2: Component-level packaging of a BGA.

Type of Interconnect	Interconnect Material	Volume per Connection (in^3)	Total Volume (in^3)	Total Volume (cm^3)	Density (g/cm^3)	Total Mass (g)
QFP	Solder paste (0.03 in. x 0.1 in. x 0.006 in.)	1.800E-05	0.0058500	0.0958643	9.63	0.9231734
BGA	Solder balls (0.03 in. diameter)	1.414E-05	0.0045946	0.0752917	9.63	0.7250589
Thermosonic ball	Gold wire bond (0.00125 in. diameter)	1.227E-07	0.0000399	0.0006536	19.3	0.0126141
Ultrasonic wedge	Aluminum wire bond (0.0012 in. diameter)	1.131E-07	0.0000368	0.0006023	2.6963	0.0016241

TABLE 1: Mass savings by eliminating external packaging.

is also achieved. Conventionally, solder serves as the attachment between a component lead frame and the corresponding CCA pad or through hole. Using IC/DT, microelectronic-grade polymers mechanically attach components to the substrate.

Thermally conductive adhesives are a good alternative to solder due to a reduction in density and lower processing temperatures. A thermoset epoxy attaches all SMD and bare die with floating backside potentials to the laminate or core. An isotropic, conductive adhesive with a volume resistivity comparable to solder mechanically and electrically attaches all die with backside potentials to the core or bond site. IC/DT makes use of wire bonds and die attach rather than solder, decreasing the volume of material per electrical connection and lowering the density of typical wire bond materials.

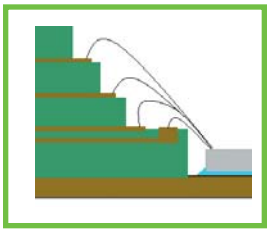

FIGURE 3: Multiple tiers for bonding ICs with high signal density.

Flexible Interconnects

Not only has analytical modeling reduced electrical attachment material mass, but the increased flexibility of the electrical interconnect further improves end product reliability. The flexibility created by using wire bonding technology as the electrical attachment process is exploited during operation in demanding mechanical environments such as vibration or mechanical shock.

A conformal coating is applied to render surfaces electrically insulating, prevent wire bond shorting and protect against moisture and contaminates. The coating also improves die shear strength and wire bond pull strength up to 900%. A silicone gel encapsulant provides vibration dampening for the wire bonds due to its low modulus in high shock applica-

tions. The gel also exhibits low levels of ionic contaminates that greatly reduce the potential for corrosion growth inside the cavities. The gel retains its low modulus over a wide temperature range due to an extremely low glass transition temperature.

Finally, a solder mask-coated copper shield is used to seal the cavities from the external environment and electromagnetic interference (EMI). The long-term reliability of a CCA is increased by using wire bonds coupled with a vibration-dampening matrix of encapsulation material to reduce the effects of wire bond resonance.

Reduced Stress from Heat and Vibration

In addition to relieving stress on the flexible connections, the cooling core also provides mechanical rigidity to reduce overall board deflection during external loading. The reduction enhances end product robustness by reinforcing the CCA for mechanical shock and vibration in its most susceptible axis. IC/DT relies on conduction to the central cooling core to remove heat from high power devices and distribute the heat evenly along the interface. The elimination of the localized heat reduces the potential for thermal component failures, increasing CCA reliability.

Using bare die reduces x/y/z dimensions, decreasing the strain on components during shock and vibration. Placing components on a centrally located, rigid core increases robustness. Lowering the z-axis component height increases the reliability of the end product.

The key to successfully implementing IC/DT is the PCB substrate layout. The physical design for IC/DT allows for increased signal density. Die are mounted in cavities to the cooling core for thermal management. Multiple tiers in cavities are used for routing high I/O devices. Multiple components placed in a single cavity reduce interconnect lengths. Multiple cavities are used for large numbers of components. Large ground and power planes are used to reduce cross-talk and directly place sensitive components.

Increased Electrical Performance

The placement of components in cavities enables wiring of high I/O density components by providing multiple tiers for bonding signal and power/ground connections (Figure 3). The tiers are comprised of exposed layer edges in the cavities with fine pitch bond pads for wire bonding signal connections. Placement of the tier bond pad is crucial for issues addressed during board fabrication as well as creating the electrical interconnects during wire bonding.

The tier wall height is minimized to allow bonding without wire-tier shelf interference. Bond shelf wall heights are kept to a minimum to shorten wire bond lengths. Cavity dimensions are also minimized to reduce distances between die and substrate tier bond pads. IC/DT design shortens wire bond lengths to improve electrical integrity of the conductor. Reducing wire bond lengths also minimizes wire bond parameters such as resistance, inductance and capacitance. ■

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This information was presented at the 2004 SMTA Pan Pacific Microelectronics Symposium; the presentation is available in the conference proceedings.