为了实现完全的过程控制和管理，建议并实行了一个可靠性、稳定性、可追踪性和可预见性（RSTP）模型。这种方法使产品开发商能够进行电子封装和焊点可靠性研究、过程鉴定、电子统计过程控制（e-SPC）、制造的实时监控以及过程和产品质量预测。本文的目的是要提供一个精简的技术工作模型并方便从产品设计到未来产品和过程质量的过渡。

Total Process Control and Management, Part I

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From reliability, stability and traceability to predictability.

To achieve total process control and management, a reliability, stability, traceability and predictability (RSTP) model was proposed and implemented. This methodology enables product developers to perform electronic package and solder joint reliability studies, product process qualification, electronic statistical process control (e-SPC), real-time monitoring of manufacturing, and prediction of process and product quality. The goal of the study was to provide a streamlined technical working model and to facilitate the migration from product design to future quality.

Two high performance packages, a flip chip ball grid array (FCBGA) and a micro pin grid array (μPGA) socket, and a product board for high-end server and desktop applications were selected. A consortium team from a package supplier, original equipment manufacturer (OEM), electronics manufacturing services (EMS) provider and software provider was established to assess the packages and solder joint reliability on a test vehicle.

μPGA Socket, FCBGA

A μPGA 959I/O socket served as an interposer with a lever-actuated feature and zero insertion force mechanism to interconnect the PGA central processing unit (CPU) to the printed circuit board (PCB).

The basic construction of the socket interposer consisted of a cover and a housing. The housing featured eutectic surface-mount area array solder balls, integral levers and a rocking latch. The cover consisted of contact cavities that accept PGA contacts and molded polarity markings. A removal tape was available on top of the cover to facilitate the pick-and-place operation.

The 1849 FCBGA was a high speed and high performance package targeting applications such as high-end graphic, high-end server, microprocessor and telecommunication routers/switchers. It utilized high-density and multiple layer organic substrates to achieve higher density

6 Factors 2**(K-P) Fractional Factorial Designs at 2 levels

	Printing Control Paramaters						Response Parameters				
Run Number	Pad Size mm (mil)	Stencil Thickness (mil)	Aperature Opening mm (mil)	Pressure (Kg)	Speed mm/sec	Seperation Speed (in/Min)	Paste Volume (mil³)	Volume Effectiveness % Actual/Theretica	Paste Height (mil)	High Effectiveness % Actual/Theretica	Paste print quality/registration (quantitative measures 1 – 5)
9	-1	-1	-1	1	-1	1					
7	-1	1	1	-1	-1	-1					
5	-1	-1	1	-1	1	1					
8	1	1	1	-1	1	-1					
10	1	-1	-1	1	1	1					
12	1	1	-1	1	-1	-1					
16	1	1	1	1	1	1					
11	-1	1	-1	1	1	-1					
13	-1	-1	1	1	1	-1					
6	1	-1	1	-1	-1	1					
15	-1	1	1	1	-1	1					
2	1	-1	-1	-1	1	-1					
4	1	1	-1	-1	-1	1					
1	-1	-1	-1	-1	-1	-1					
3	-1	1	-1	-1	1	1					
14	1	-1	1	1	-1	-1					

DOE Level	Pad Size mm (mil)	Stencil Thickness (mil)	Aperature Opening mm (mil)	Pressure (Kg)	Speed (mm/sec)	Seperation Speed (in/Min)
-1	16.5	5	1.1 pad	9	20	Low
1	20.9	6	1.3pad	15	70	High

TABLE 1: Paste printing optimization.[1]

2 factors, 3 levels, 3**(2-0) full factorial design

	Thermal Control Paramaters		Response Parameters			
Run Number	Time above 183°C Sec	Max Reflow Temperature (°C)	Package Wrapage Shadow Moire/RVSI (mil)	Solder ball Diameter by 5DX (mils)	Solder Quality /Wetting (Qualitative measure)	Standoff from substrate/ (mil)
1	-1	-1				
2	-1	0				
3	-1	-1				
4	0	-1				
5	0	0				
6	0	1				
7	1	-1				
8	1	0				
9	1	1				

DOE Level	Time above 183°C Sec	Max Reflow Temperature (°C)
-1	60	200
0	100	210
1	150	220

TABLE 2: Thermal profile optimization.[2]

I/O interconnection, better signal integrity and improved reliability on the PCB level.

The integrated circuit (IC) chip was fabricated with high lead bumps, and then the flip chip was mounted onto the organic substrate. Underfill was applied to the gap between the IC and organic substrate to lock the IC chip and its high lead bumps. The flip chip package consisted of a copper stiffener to enhance package stability and reduce substrate warpage and a nickel-plated copper lid to ensure high thermal conductivity. The ball pitch of the package was 1.0 mm with a full array of 1849 pins.

Two types of substrates—Substrate A (7 layer) and Substrate B (9 layer)—were used. Core layer stacked up/lamination provided the flexibility for routing high I/O devices from the die center and reducing layer count.

Test Vehicle

To assess the solder joint reliability under the package/substrate and optimize the process window, test vehicles were designed with a daisy chain (DC) structure.[1] The DC of the package was separated into die level and substrate level so the integrity and continuity of these two levels could be traced at the same time. Eight FCBGA with DC were laid out on the test vehicle (TV)[1], and two µPGA sockets were laid out on another TV[2] to trace the reliability of the package and solder joint.

Model I: Reliability

To determine the influence of controlled variation from the process to the reliability of the package in a systematic approach, a package reliability and process optimization model was initiated via the design of experiment (DOE) method.

Paste Printing Optimization

Pad sizes with five other process variables were optimized by using a fractional factorial design in a two-level DOE as shown in Table 1. The solder volume was measured, and printing effectiveness was calculated by comparing the theoretical volume from the stencil thickness and aperture geometry. Similarly, the paste height printing effectiveness was calculated.

With the variation of printer mechanisms and process direction, the analytical approach proposed from a previous study[2,3] was used to reveal the correlation of solder volume/printing efficiency to the printing and squeegee directions. The paste volume from the solder paste inspection system was formatted into the pin orientation; data were then statistically analyzed to see significances in the distribution.

Thermal Optimization DOE

The thermal profile for the package and TV were derived by using a three-level DOE (Table 2). The DOE level for control was selected to accommodate the thermal specifications of the package and process equipment.

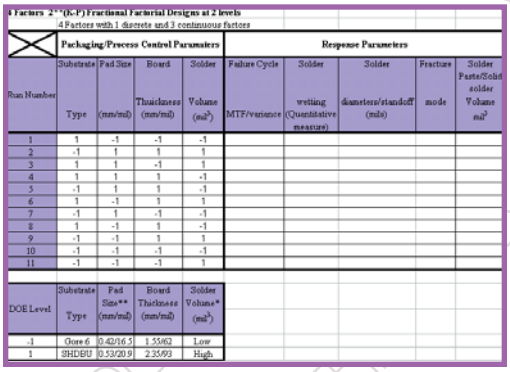
The solder ball size and circularity at the following three levels were scanned as an important response parameter: (1) package pad and solder ball interface, (2) center of the solder ball and (3) interface of PCB pad and solder ball. The standoff of the package was estimated by measuring at the left, middle and right-hand side of the diagonal of the package on the cross section sample, as well as by laminography. Optical microscope and SEM/EDX were used to determine the solder wetting and microstructure integrity.

Package Realiability, Process Optimization DOE

A package with two types of substrate construction, material properties and three other PCB and process control variables was studied in a four factor fractional factorial design with two levels as shown in Table 3.

Data collection devices and failure analysis techniques were utilized in the process and in the assessment of the

TABLE 3: Package reliability assessment and process optimization DOE.[2]



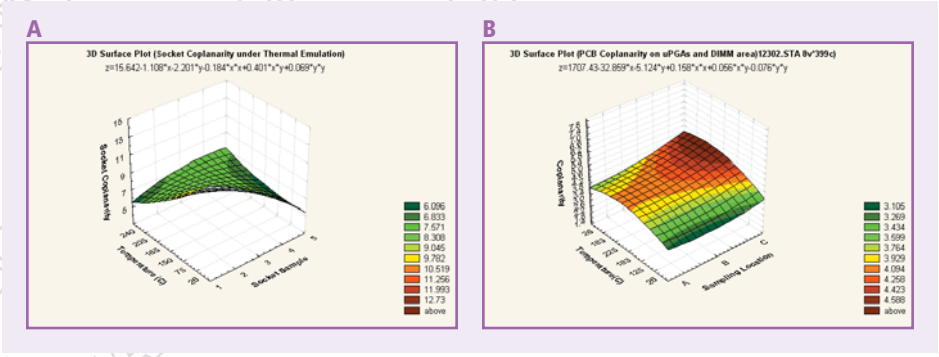


FIGURE 1: Three-dimensional surface plot of package warpage of µPGA (a) and flatness of PCB (b).

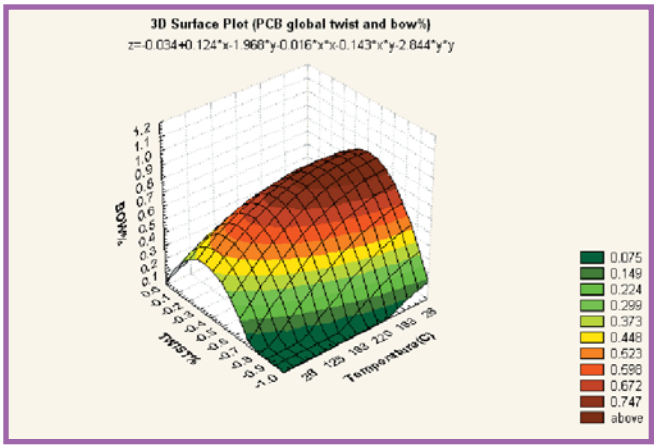


FIGURE 2: Surface plot of twist and bow of the PCB on a global scale.

fracture mode of the solder joint and package in accelerated thermal testing (ATC). The hardware setup for the reliability oven and real-time monitoring followed IPC standards, SM-785[5] and 9701.[6]

Reliability Testing

Three types of reliability tests—interconnect stress test (IST), repeated torsion test and ATC—were conducted to assess the via integrity on the TV and solder joint reliability. The failure cycle and fracture mode were used as a response to optimize the package substrate construction and process window.

The IST was performed on the TV to assess the reliability of plated via and embedded trace connections in the PCB per IPC-TM-650 Number 2.6.26. Two test coupons for IST were laid out along the wide side of the TV. One coupon was used as PCB incoming quality analysis, and the second coupon stayed with the TV through the assembly process to quantify the via life/integrity and degradation due to the impact of mechanical handling, thermal process and electrical test. The test coupon with the daisy chain via structure tracked the net resistance change during the thermal cycle. The specific resistance/temperature level was designed to be just above the glass transition temperature of the substrate (150°C).

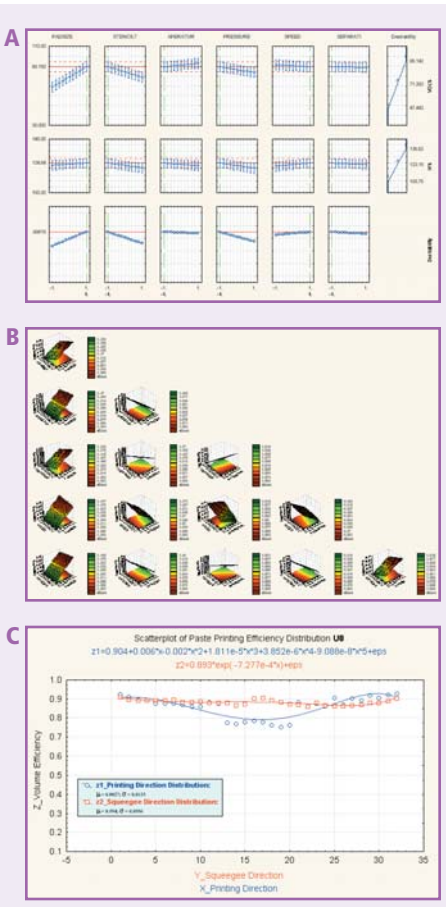


FIGURE 3: DOE grid search (a) and response profile (b) for paste printing optimization. Scatter plot of printing efficiency of two µPGA sockets along printing and squeegee directions (c).

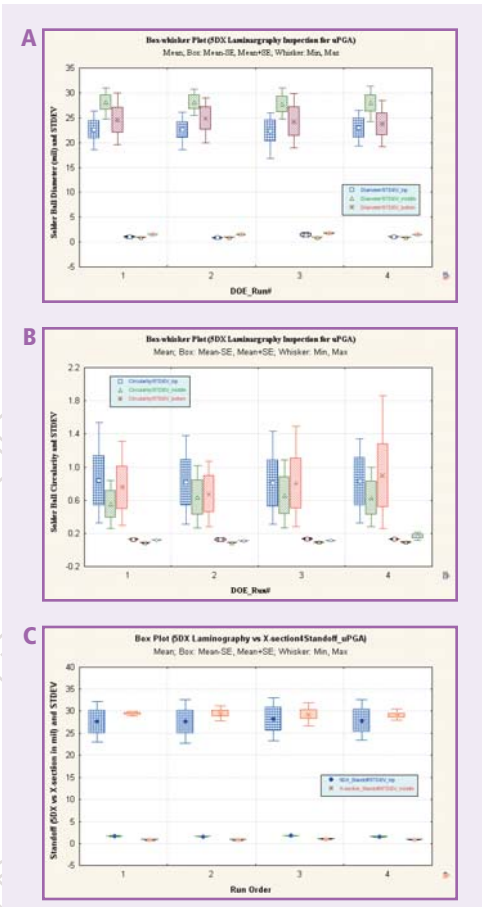


FIGURE 4: Solder ball diameter (a) and circularity (b) of a µPGA socket by laminography, and solder ball average standoff and standard deviation measurement by laminography and cross section (c).

A device similar to the mechanical deflection system (MDS) was used in a second DOE as a test method to screen the responses for the solder joint reliability.[7] This tester used coupled torsion forces to induce repetitive in-plane shear and out-of-plane tensile forces on the TV to simulate mechanical stress on the solder joints. The applied repetitive torsion force changed its direction and magnitude as the TV reached each half cycle.

ATC with a 10-min. ramp and dwell and 10°C/min. ramp rate in the range of 0°C to 100°C was conducted to assess the solder joint reliability. A real-time event detector was used in the single zone test chamber for ATC testing so that intermittent high resistance in the DC could be captured. The test duration was 63% cumulative failure or 6,000 cycles, whichever condition occurred first. The basic ATC test, real-time monitoring and oven setup followed the Solder Joint Reliability Test Standard[6] and IPC-SM-785.[7]

Process, Solder Joint Quality

Quality of the solder joint and process window was derived from reliability tests; visual inspection and package warpage and PCB flatness; x-ray inspection; dye penetrant test and metallurgical cross section.

Visual inspection was performed on the periphery solder joint of the FCBGA package and socket by using an optical microscope. The assessment of the quality of solder joint was the major purpose of this test. The focus was on assembly and rework defects such as solder bridging, insufficient solder, ball misalignment and cold solder joints. The Shadow Moiré technique was used to inspect the PCB flatness and FCBGA and µPGA socket warpage under the temperature profile—26, 125, 183, 225, 183, 26°C—to emulate the thermal impact in the early stage of the package and reliability study. Surface mapping was plotted to show the coplanarity, twist and bow of the PCB and coplanarity of the packages.

The solder joints of all packages on the test vehicle were examined using a transmission x-ray to detect possible solder defects in solder joints on the inner rows. Laminography x-ray inspection was also performed on packages. The diameter and

circularity at the PCB side, package side and center of the solder ball under the package were measured.

A dye penetrant test was performed on both first pass and reworked TVs after reliability testing. The test procedure and failure mapping were specified in an earlier study.[7] Statistical analysis was performed after the failure mapping, and criteria of the process window were concluded.

All cross sections were finely polished down to 0.05 µm and chemically etched. All cracks, intermetallic compounds (IMC), solder alloy structure and wettings were examined using an optical microscope and scanning electron microscope (SEM). The chemical compositions of the solder alloy and IMC were also identified with energy-dispersive x-ray spectroscopy (EDS) and x-ray fluorescence.

Model II: Stability

To establish a robust manufacturing process, a few major process steps should be implemented. Through these steps, the yield and defects per million opportunities (DPMO) for a product will be in control and migrate to a higher statistical standard.

Process Window Matching

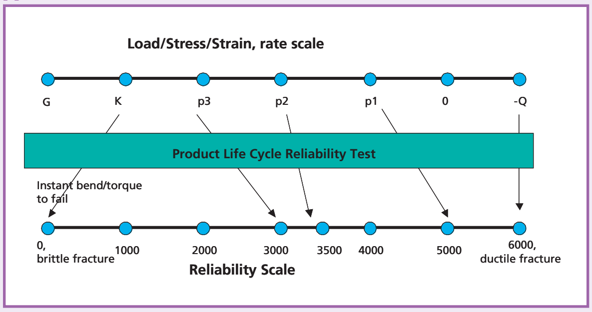
The process windows for paste printing and thermal reflow, as well as the profile for mechanical parts derived from Model I: Reliability, were process-matched. As shown in Model I, all major intrinsic process variables such as paste volume and reflow dwell were derived and optimized along with machine-specific parameters such as printing pressure and reflow conveyor speed. These intrinsic process variables enabled the developer to move the optimal window for a specific product to a different surface-mount line by performing a simple matching process by using statistical indexes.

IQA Screening

Figure 1a and b show the PCB flatness and µPGA socket under emulated temperature profile by Shadow Moiré. The co-planarity is defined as the difference between the maximum to minimum z-axis height of the package along the diagonal line. As shown in the surface plot, the higher the temperature, the smaller the difference in the thermal characteristic of most polymer material. Based on the data, socket flatness variation is larger as compared to the PCB specification.

Since high temperature is more critical for solder interconnects, the large flatness variation may not be an issue. Although the stress relaxation of the solder joint and its influence to reliability are unknown, the system cooled down to a lower temperature. Figure 2 shows the twist and bow of the PCB at various temperatures. The maximum percentage of twist and bow was in the range of 0.7 to 0.84 with respect to the diagonal or side length. Overall PCB flatness at the local socket pad area and global location fulfilled general requirements. Laser scanning was performed on both types of packages for the coplanarity of the solder bump.

A



B

	Control Parameters		Response Parameters					
Run Number	Loading Speed ds/dt	Deflection z	Failure Cycle 63%CF/ variance	Strain and rate εx, εy	Solder wetting (Quantitative measure)	Solder diameters, circularity, standoff (mils)	Fracture mode/ configuration	etc
1	-1	0						
2	0	1						
3	1	-1						
etc								

DOE Level	Loading Speed ds/dt	Deflection z
Time zero	Load to fail,	from left
-1	p1	z1
0	p2	z2
1	p3	z3

FIGURE 5: Strain/rate correlation to the reliability scale (a) and DOE implementation approach from proactive intrinsic variables, loading speed and deflection to solder joint reliability (b).

Paste Printing

Figure 3a and b show the optimized process window that derived from the statistical grid search and response profile. Five control variables demonstrated strong correlation to the response as indicated from multiple regression analysis. Separation speed showed little influence to the paste volume and height due to possible factors such as aperture finish. Three major indexes for the statistical analysis—probability plot of the residue, prediction and residue, and a Box-Cox plot—indicated that the data matching was robust.

A three-dimensional trace plot and surface plot were generated based on printing efficiency on all I/O. A two-dimensional scatter plot of the average printing efficiency along the x printing direction and y squeegee direction was generated (Figure 3c). A 5% small variation of printing efficiency occurred along y squeegee direction on U8 and U13 as expected. Consistent data distribution along the squeegee path was also observed. The small variation was rationalized due to the squeegee being supported by the rails in the direction of y. A large 15% paste printing variation in the printing depth direction x was found for both U8 and U13. The central dip was a normal response for the compliance of the PCB to the printing pressure.

Other Measurements

The solder joints of the FCBGA and µPGA were inspected under transmission x-ray and optical microscope inspection. No solder joint abnormality occurred.

Solder diameter and circularity at three levels were studied by using X-Ray Laminography (Figure 4a and b). The diameter of the solder joint at the middle showed less variation and higher average value due to the fact that wetting of the solder was limited by the pad size at top and bottom and characteristic of the pad surface.

On the other hand, wetting at the PCB pad had a higher circularity value due to the definition of pad geometry. However, the variations of the data are larger at both the top and bottom levels, again due to the surface characteristic of the pad.

Figure 4c shows the standoff of the µPGA along the diagonal line by two methods, laminography and cross section. A consistent trend occurred in both data collection methods. Data range dispersion was about 25% by laminography as compared to 5% by the cross section method. However, the centerlines of data distribution were very close by both methods. Standard deviation also showed consistent pattern with 5% deviation. This consistency of standoff across the diagonal length has positive contributions to solder joint reliability.

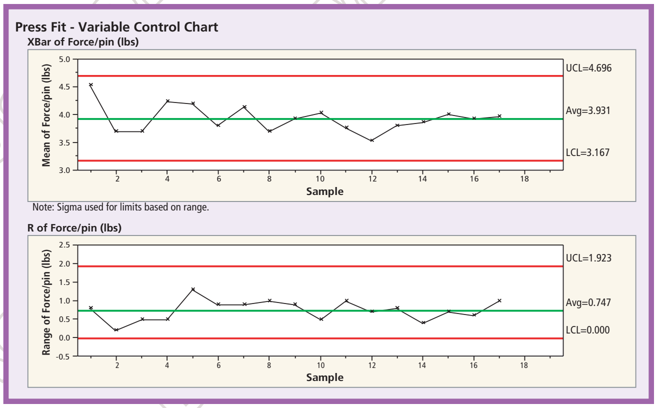


FIGURE 6: X-bar and R control charts of VHDM insertion force per pin.

Mechanical Stress Monitoring

Mechanical stress from various sources is a major concern for solder joint reliability. Strain gauges have been widely used in detecting the strain change on the PCB as well as package surfaces during and after a specific process. To avoid instantaneous cracking at the BGA joint, the current strategy is to reduce as much strain/rate as possible, although this reduction may just delay the instantaneous type of failure to the long-term fatigue type of failure. Therefore, a logical resolution is to establish the correlation of loading speed and deflection to the reliability scale as illustrated in Figure 5a and b.

Process Control to Statistical Run

With the process window derived and an effort made to match these intrinsic variables, the large sample size in the new product introduction (NPI) and process qualification stages allowed the process developer to establish basic statistical indexes with good confidence. Figure 6 shows an example of x-bar and R control

charts of a VHDM insertion into a product board. With specific quality control limits defined, the control chart monitored the insertion force (lb/pin) in time series throughout the product assembly history. Major statistical indexes were calculated on paste volume, solder diameter and circularity, standoff, epoxy volume for heatsink and shear strength. All these efforts paved the way to achieve the total data-driving process control and management.

The general rules for quality process control are based on common sense and statistical reasoning. Data outside the control limit—six in a row and/or eight in a row on one side of the centerline—are referred to as out of control. By assuming three rationales—the data follow a trend of normal distribution, consecutive samples are independent and not correlated, and a process is in control—the probability of any sample mean in an x-bar control chart above or below the centerline is equal to 0.5. Accordingly, the probability that nine consecutive samples will fall on the same side of the centerline is equal to 0.5**9 = 0.00195. Note that this number is approximately the probability with which a sample mean can be expected to fall outside the three-times sigma limits. Therefore, these rules are used in the process qualification as the point at which quality alert and engineering resolution should be prompted. ■

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Part II of this article will be featured in the May issue, and Model III (Traceability) and Model IV (Projection) of the experiment will be discussed.

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