

Do you like news and articles like this?

Then, get it from the **ORIGINAL** source ... <u>PCB UPdate</u> ... the semi-monthly e-mail newsletter produced by **Circuits Assembly** and **PCD&M** and circulated to over 40,000 readers.

CLICK HERE TO READ THE ARTICLE YOU REQUESTED

Process Control



为了实现完全的过程控制和管理,建议并实行了一 个可靠性、稳定性、可追踪性和可预见性 (RSTP) 模型。这种方法使产品开发商能够进行电子封装和 焊点可靠性研究、过程鉴定、电子统计过程控制 (e-SPC)、制造的实时监控以及过程和产品质量预 测。本文的目的是要提供一个精简的技术工作模型 并方便从产品设计到未来产品和过程质量的过渡。

Total Process Control and Management, Part II

Dr. Paul P.E. Wang, Jorge Martinez-Vargas, Dinesh Gill, Ramamoorthy Ganapathy Iyer and Dan Kauss

From reliability, stability and traceability to predictability.

Part I of this article was featured in the April issue, and Model I (Reliability) and Model II (Stability) of the experiment were discussed.

Model III: Traceability

As a consequence of the Internet bubble bursting a few years ago, overcapacity of human resources and equipment, overstocked inventories and low buying incentive in the market have forced the electronics manufacturing industry to increase profit margin by reducing operating costs. Projects based on statistical process control (SPC) and Six Sigma methodologies are being initiated in every aspect of corporate life to overcome the plateaus of quality improvements from design through engineering to manufacturing.

Many companies seem to progress through similar learning curves to achieve Six Sigma quality (Figure 1a). Following are descriptions that summarize a few references^{1,2,3} on overcoming quality plateaus and the path to achieving Six Sigma quality, or 3.4 defects per million opportunities (DPMO).

Embryo Stage: Low-Hanging Fruit

Quality improvement as a result of Six Sigma processes may be achieved early and rapidly by using relatively unsophisticated methods. Implementing and auditing well-defined procedures, while improving designs using design for manufacturing (DFM) and well-known concurrent engineering principles, provide much of the benefit.

The first plateau quickly becomes apparent, especially when DFM guidelines and reliability data are not sufficient to achieve high quality. Some commercial software tools as shown in Figure 1b support Six Sigma by ensuring all defects are counted and charged back to the responsible process. Pareto charts, measles charts and fishbone diagrams are typically automated to facilitate the failure analysis and isolate the root cause in a timely manner.

SPC, DOE

After significant time has been spent at the first plateau, with the quality level reaching Four to Five Sigma in some cases, these preliminary methods may not be able to achieve Six Sigma levels. This knowledge has caused a back-tobasics program to be initiated in many sectors, with renewed emphasis on more sophisticated quality improvement methods such as SPC and Design of Experiments (DOE).

As shown in the first two models presented in Part I (April 2004, *Circuits Assembly*)—Reliability and Stability—these methodologies have been applied in an electronic and solder joint reliability study, process optimization and product process qualification with great success. Generic statistical tools have been widely used for firstlevel process optimization and reliability tests in such applications as underfill material and under



FIGURE 1: The learning and achievement plateaus on Six Sigma (a) and commercial defect entry and analysis tools (b).

bump metallization material composition and thickness. These off-the-shelf statistical tools are also being used on solder joint reliability and assembly process optimization, including paste printing, thermal reflow and solder joint and process quality testing.

Moreover, software developers are also proactively involved with equipment vendors to support communication protocols to provide the needed quality data. The SECSII/GEM options now available on many machines resulted in a large part due to these efforts. These new protocol development-working groups such as IPC CAMX also help to ensure that the new standards are workable and are implemented quickly.

Failsafe (Pokayoke)

Another type of process control deployed to overcome this quality plateau is the pokayoke, or the failsafe. This method performs 100% inspection both before any raw material moves into design/assembly and immediately after the process. The essential action is to stop the machine or at least warn the operator if a defect is found. This concept helps to ensure a clean start after incoming quality assurance (IQA) and to conduct extensive in-process inspections, which are proactively built into Model I (Reliability) and II (Stability) as independent control variables and dependent response parameters.

A part verification system can be applied in proactive IQA for surface-mount parts and reels before the pick-and-place process. A wireless barcode scanner can scan the machine feeder slot, the new reel and the operator, if so configured. A warning will be displayed whenever the part scanned is not correct according to the machine program.

e-SPC Manufacturing

Optimal quality control and management of quality functions for a product from design through engineering to manufacturing is aided with traceability information. This function will use existing models as mentioned above to record the field quality data, cross-check against predetermined statistical run rules and provide real-time monitoring and reporting of the sta-



FIGURE 2: An example of an e-SPC manufacturing information network.

tus to process management with Web accessibility. Furthermore, this quality module will provide vital information feedback to the product owner as well as prompt the quality/process engineering team for immediate resolution.

As an example of how to achieve this optimal goal, some commercial software products reportedly use a number of software modules to monitor utilization based on the SEMI E-10 standards, monitor quality using SPC charts and enable alarming of out-of control processes. These modules can interface with both GEM- and non-GEM-compliant machines to collect vital data, store it in a database and display information to the users. These real-time and historical charts and reports can be viewed via monitors on the production floor or via a Web reporting tool from any networked computer in the enterprise.²

Other organizations have also built this capability on top of their shop floor tracking systems to achieve the optimal information network among suppliers, electronics manufacturing services (EMS) providers and original equipment manufacturers (OEMs), as shown in Figure 2. This framework and methodology will make sense only if the building blocks have a universal



FIGURE 3: Package/solder joint/PCB system model construction (a); four-point bending fixture schematic (b)⁴; and the corresponding upside down test vehicle for the four-point bending test with imposed boundary conditions (c).

language that fulfills an industry protocol. However, this approach, in general, has had good compatibility between data collection devices and equipment.

Model IV: Predictability

As the electronics industry continuously striving towards miniaturization and high signal integrity performance, packages, such as flip chip ball grid arrays (FCBGAs) and chip-scale packages (CSPs), and high-density printed circuit board (PCB) layout have vital roles in the competitive product market. Study of thermal and mechanical cycling tests on solder joints shows that factors such as solder volume, pad geometry, standoff and PCB thickness have great contribution to the reliability of the system. However, the brittle fracture of solder joints under external force in electrical test, mechanical process and PCB handling and its correlation to reliability are areas that have not been thoroughly studied. This lack of study is due to the difficulty of statistical control of sample characteristics in DOE and product development cycle and cost.

Therefore, the objectives of Model IV were:

1. Use a numerical approach such as finite element method (FEM) to predict the physical response of the package/solder joint/PCB when a predetermined boundary condition (BC) was imposed upon this system.

2. Create a FEM model to emulate a four-point bending experiment⁴ on an over 100 I/O, 0.8 mm pitch BGA on an over 90 mil thick PCB with orthotropic material property. The material properties of the silicon die, molding compound, substrate and solder mask were defined. The strain response under these loading conditions was analyzed.

3. Derive Von Mises stress and strain at the solder bump to PCB pad interface, and compare data to the strain gauge result.

Statistical Database to Computer Modeling

The unit lattice of the model, including solder bump, copper pad and solder resist, was created as an essential building block of the model as shown in Figure 3a. Engineering assumptions for the computer modeling were as follows.

· Assume uniform linear elastic material property. Two eutectic phases, α and β , and their strengthening mechanisms against external mechanical brittle fracture or thermal/mechanical cycling on fatigue failure were not considered.

• Simplify the package internal construction and keep the focus on the interface to the solder bump and PCB surface response under bending.

· Simplify the distributed copper trace layout in the general circuit design to layers of copper intertwined with FR-4 laminate composites.



Maximum Von Mises strain contour plot at the solder bump to package substrate interface (a) and close-up (b). • Create the lattice of solder geometry with simplified surface curvature to accommodate the eightnode Solid 45 element geometry.

• For this exercise, apply a simple one cycle of four-point bending to the system.

Solid 45 element was used for the three-dimensional (3-D) modeling of solid structures. The element was defined by eight nodes having 3 DOF at each node, translation in x, y and z directions. This element had plasticity, creep, swelling, stress stiffening, large deflection and large strain capability.

A standard four-point bending test fixture was setup as shown in Figure 3b. The corresponding package/solder ball/PCB system with loaded boundary conditions is shown in Figure 3c. The outer support span was 0.756 in., and internal span

was 0.378 in. The displacement constrain on nodes at the outer span was Uy=0. A displacement load with value Uy=+0.125 in. was applied on nodes on the bottom side of the test vehicle (TV). All the nodes on the symmetry surfaces were constrained as Uz=0 or Ux=0.

The Von Mises total strain contour plot, as shown in Figure 4, indicated that the maximum strain location at the solder joint to the package substrate interface occurred at nodes 1572, 10096, 10095, 10403, 11020 and 11328. Table 1 shows the equivalent

principal stresses at the solder ball to package substrate interface. By studying the Von Mises stress and strain in other I/Os at the package substrate to solder ball interface, the value of the outer row was consistently larger than the inner row at this interface (Table 2).

Figure 5 shows the Von Mises stress contour plot. The maximum values were located at the solder joint to PCB interface. Overall, the stresses at the interfaces at nodes 11185, 10874, 10569, 10261, 9953 and 393 were very consistent with the value of 1.05E+06 Psi. Based on few available data from strain gauge measurement, the actual value was approximately 20% larger than the FEM output at node 16315. The tensile and shear yield strength of the eutectic solder were in the range of 10-20 Mpsi.

Eutectic vs. Lead-Free Solder

Material property of the solder was modified to lead-free in the SnAgCu alloy,⁵ and the above analysis was benchmarked. Figure 6 shows the correlation of Von Mises

Von Mises Stress/Strain at solder ball to package substrate interface										
Node	572	10096	10095	10403	11020	11328				
Von Mises Strain (in/in)	0.14715	0.15362	0.10571	0.10534	0.12839	0.14593				
Von Mises Stress (Psi)	47005	39151	49543	39016	47553	46856				
Von Mises Stress/Strain at solder ball to PCB interface										
Node	11185	10877	10569	10261	9953	393				
Von Mises Strain (Psi)	1.05E+06	1.05E+06	1.05E+06	1.06E+06	1.05E+06	1.03E+06				
TABLE 1: Equivalent principal stresses at the solder ball to package substrate interface.										

	Outer Row	2nd	3rd	4th	5th	Inner Row			
Node	572	8559	8867	9175	9483	9791			
Von Mises Strain (in/in)	0.098972	0.06915	0.052536	0.038066	0.023788	0.013468			
TABLE 2: Von Mises strain variations from outer row to inner row to show DNP cor-									

 TABLE 2: Von Mises strain variations from outer row to inner row to show DNP correlation.

> at the ball to PCB and ball to package substrate interfaces with eutectic solder and lead-free solder. Similar DNP correlation to the strain and consistent stress levels across both interfaces were observed. With the same external force and similar strain on both models, lead-free solder showed higher Von Mises stress for module of elasticity.

> Table 1 shows consistent nodal deflection of 0.15 in. for those nodes adjacent to the outer row of the solder ball under 0.125 in. displacement load applied at 0.189 in. distance away from the

FIGURE 5: A Von Mises stress contour plot shows the maximum at the solder to PCB interface. The black circle shows where the strain gauge was attached.



FIGURE 6: Von Mises stress at the ball to PCB and ball to package substrate interfaces with eutectic vs. lead-free solder (under four-point bending forcefield).

edge of the package. Von Mises stress and strain values in both cases were much lower—3.4% than the yield strength. Therefore, no failure concern existed under 0.125 in. of displacement, although accumulative strain energy over time might go over the limit and cause fatigue failure if the system is under cycling thermal or/and mechanical load.

Conclusion

To achieve total process control and management from design to manufacturing, the Reliability, Stability, Traceability and Predictability (RSTP) Model was proposed and implemented. To assess the reliabil-

ity of the electronic package and solder joint and identify the process window in the early stage of the product design cycle, a few test vehicles with daisy chain construction and product features were designed. DOE was extensively used from process development to package reliability assessment.

A process qualification model was initiated to derive the control limit of various processes, including paste printing, pick-and-place, pre- and postreflow quality, press-fit, inspection and heatsink attachment. Techniques were implemented to check the responses and monitor solder wetting quality and chemical composition. Strain gauge was used to assess the strain response in various mechanical processes to ensure that general guidelines were met.

To achieve the final step of total process control and management, certain software and processes that can link data from inspection devices to shop floor tracking systems were under evaluation. Web access provided by e-SPC and manufacturing capabil-

ities were embedded in the software to provide out of control process alarm notification, statistical control monitoring and equipment utilization feedback. This e-SPC integration effort not only provided real-time alarm and Web-based remote monitoring, but it also provided traceability for failure analysis, early process resolution and process control of product quality projection.

Finally, FEM was used as an approach to build Model IV: Predictability and to emulate the physical characteristics of the package/solder joint/PCB system under mechanical force. Stress responses of the system were studied. Under force, Von Mises stress and strain at the solder ball to package substrate and the solder ball to PCB interfaces were derived. Responses of both eutectic and lead-free solder under predetermined boundary conditions were compared.

References

- Overcoming the Current Quality Plateau, Michael Motherway, SMTA International conference, Chicago, IL, September 25, 2002.
- e-Manufacturing Software for Product and Process Realtime Monitoring, Hersh Kohli, Rajan Chatterjee, Dan Kauss, SMTA International conference, 2001.
- Increasing Operation Margins in a Down Economy: Case Studies in SMT Production Monitoring Software & Applications, Dan Kauss, APEX conference, 2003.
- Monotonic and Cyclic Bend Test Standard, Celestic / Cisco / Intel / Solectron / Sun Working Group, *IPC MCB-01*, Rev.1, June 10, 2003.
- Properties of Lead-Free Solders, Database for Solder Properties with Emphasis on New Leadfree Solders, Release 4.0, NIST and Colorado School of Mines, February 11, 2002.

Acknowledgments

The authors wish to acknowledge the following people: Mark Turnlund, Margaret Hsu, Jamie Scott, Ken Kochi, Livia Hu, Hank Ching, Gary Huang, Kim Hyland, Sundar Sethuraman, Michael Motherway, Hersh Kohli, Ranjan Chatterjee, Dr. Sheri Sheppard, David Michael Pierce, Heather McCormick, Jim Chow, Dave Ellison, Sameer Ahmed, Hiroshi Tabuchi, Vincent Hool, Narayanan, Harvey Fletcher, Patricia Lim, Vincent Madhavan, M.S Lee, Nad Rajan, Rahmad, V. Subramanyam, SK Tan, Fok Ee Ling, Dominic Lo.

Dr. Paul P.E. Wang (email: Pauchiu.Wang@Sun.com) and Jorge Martinez-Vargas are with Sun Microsystems, Inc., Santa Clara, CA. Dinesh Gill and Ramamoorthy Ganapathy Iyer are with Solectron Corp., Penang, Malaysia. Dan Kauss is with Motorola Inc., Schaumburg, IL.

The original version of this article was originally published in the 2003 SMTA International Proceedings.