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晶片级芯片尺寸封装（CSP）是单独的硅芯片，其中包含一个薄膜再分配层，以标准的表面贴装间距对装置布线。晶片级CSP的密间距性质常常要求印刷电路板的布线利用导通孔技术，获得完整功能。晶片级装置的长期可靠性也是必须解决的问题。本文讨论用于在传统印刷电路板焊盘以及盘中导通孔结构上组装46输入输出、0.75毫米间距的晶片级装置的程序。各种组装构成的可靠性在空气对空气热循环中予以评估，并使用威布尔分析进行对比。

Assembly and Reliability of a Wafer-Level CSP

Michael Meilunas and Parvez Patel

An experiment reveals that wafer-level devices can be assembled in high yield using standard surface-mount practices.

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Chip-scale package (CSP) technology continues to push the limits of miniaturization on both the package and printed circuit board (PCB) level. Wafer-level CSPs are individual silicon chips that contain a thin film redistribution layer to route the devices to standard surface-mount pitches. The packages are small, light and available in fine-pitch formats with I/O counts ranging from 4 to over 200.

The fine-pitch nature of the wafer-level CSP often requires that the PCB routing incorporate via technology to fully exploit the functionality of the device. Although dog bone via structures are preferred, the density of the routing may require via-in-pad technology to accommodate the wafer-level package.

The long-term reliability of wafer-level devices is a concern that must be addressed. Direct chip attach, or flip chip assembly, is a proven technology that is widely used. Wafer-level devices are, more or less, large flip chips. However, flip chips rely on an underfill to improve the mechanical and thermal fatigue resistance of the package. If a wafer-level CSP is to be used as a drop-in replacement for a traditional CSP, an underfill material cannot be used.

This article discusses the processes used to assemble a 46 I/O, 0.75 mm pitch wafer-level device on conventional PCB pads and on via-in-pad structures. The reliability of the various assembly configurations was assessed in air-to-air thermal cycling and compared using a Weibull analysis.

Reliability of Wafer-Level CSPs

Compared to conventional CSPs, wafer-level CSPs are less likely to experience popcorning, die-substrate delamination and other moisture-induced defects. However, the mechanical and thermal behavior of a wafer-level CSP is dominated by the silicon die. Therefore, a wafer-level CSP will typically have a coefficient of thermal expansion (CTE) that is much lower than a traditional overmolded CSP. The wafer-level CSP is also stiffer and less compliant to thermally and mechanically induced stresses than most CSP designs.

Package Description

The device used for this assembly and reliability experiment did not require underfill. The package pads were routed to a 0.75 mm pitch using CSP-size balls. This device was intended for memory applications such as flash, DRAM, EEPROM and SRAM.

The device was a true wafer-level package as it used standard semiconductor processing equipment to produce a thin-film redistribution layer and a wafer-level ball attach technology. The package contained a two-layer polymer dielectric system of benzocyclobutene (BCB) and a thin film solderable redistribution layer of Al/NiV/Cu.

The device contained 46 solder bumps distributed in an area array (6 by 8 pattern), depopulated at the center. The package was rectangular in

shape with physical dimensions of 0.317 in. x 0.246 in. and a thickness of 0.0438 in. (from the top of the die to tip of the bump). The silicon die had an overall thickness of 0.027 in. and was attached to a 0.0003 in. flex layer. The Sn/37Pb solder bumps had an unassembled diameter of 0.0215 in. and a height of 0.0165 in.

The measured CTE of the package was approximately 4.5ppm/°C. The package was rigid and did not warp upon heating or cooling.

Test Board

The test board used in this experiment was a 0.041 in. thick, double-sided FR-4 substrate with four signal layers (two surface and two internal). The board was finished with an organic solderability preservative (OSP) to protect the copper pads.

The glass transition temperature of the board was 175°C, and the CTE was measured to be approximately 16 ppm/°C.

Six land array patterns were utilized in the experiment. Three of the patterns contained standard, non-solder mask-defined (NSMD) pads with diameters of 0.011, 0.013, or .015 in. The remaining three patterns also contained NSMD pads with 0.011, 0.013 or 0.015 in. diameters, but each pad contained a 0.005 in. diameter (nominal) via. The via-in-pad structures were used to route the surface signal layer to an internal signal layer. The via-in pads were unfilled. Figure 1 contains images of the via-in-pad structures. Via misregistration is observed in the figure.

Test Plan

The main objectives of the experiment were to:

- investigate assembly issues concerning the wafer-level CSP
- compare solder paste assembly to flux assembly and effect on solder joint reliability
- determine the feasibility of assembly on via-in-pad land patterns and compare the solder joint reliability to conventional NSMD pad connections
- evaluate the effects of PCB pad size on the solder joint reliability for both conventional and via-in-pad structures.

FIGURE 1: (left) Top view of 0.015 in. pad with 0.005 in. via and (right) side view of 0.011 in. pad with 0.005 in. via.

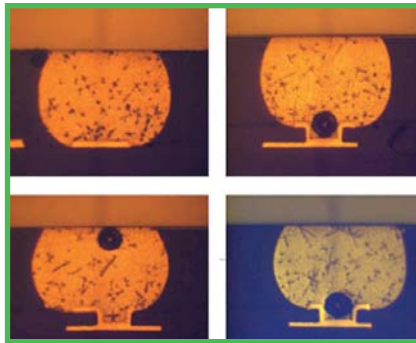

FIGURE 2: Cross sectional images of solder joints on conventional pad and via-in-pad structures.

Assembly

The wafer-level devices were assembled in two sets. Set 1 assembly followed a traditional CSP assembly process, while Set 2 assembly involved standard flip chip practices. A single reflow profile was developed for both assembly processes using a forced convection oven.

Prior to assembly, the wafer-level devices were baked at 125°C for 12 hours. This practice removes excess moisture from the packages and prevents popcorning and delamination. The test boards had been stored in sealed packages and were not baked prior to assembly.

Set 1 assembly utilized a no-clean, type IV Sn/37Pb solder paste with a 90% metal content. The paste was printed over the PCB pads using a stencil constructed from 0.005 in. thick stainless steel foil. Polyurethane squeegees with a durometer hardness of 95 positioned at an angle of 60° were used to apply the paste to the test boards. A print speed of 15 mm/sec. and a print pressure of 0.49kg/in. resulted in excellent print deposits. The wafer-level devices were then placed on the PCB and reflowed in the forced convection oven.

Set 2 assembly was performed by applying flux to the wafer-level devices through the use of a thin film applicator (TFA). The devices were dipped into a 0.0045 in. thick layer of no-clean tacky flux prior to placement. Once the devices were placed, the assemblies were run through the forced convection oven. No underfill was applied.

Reflow was performed using a standard ramp-soak-ramp profile. The test boards and wafer-level devices were heated from room temperature to 165°C at a rate of 1.5°C/sec. The assemblies then dwelled at 165°C for approximately 140 seconds to allow for solvent evaporation and flux activation to occur. The assembly temperature was then increased to a peak of 220°C at a rate of nearly 4.0°C/sec. The assemblies were then cooled to 85°C (exit temperature) at an average rate of 2.0°C/sec. This reflow profile resulted in a time above liquidus (183°C) of approximately 47 sec. and required 6m45s to complete. A reduced oxygen atmosphere was used throughout the reflow operation. Nitrogen gas (N_2) was pumped into the oven so that the oxygen content was below 50 ppm.

Post-Assembly Operations

Electrical, visual and x-ray inspection techniques were employed to qualify the wafer-level assembly process.

Probe testing with a multimeter indicated that all assemblies were electrically good. The analysis also indicated that the various assembly combinations (PCB pad dimensions, paste or flux) had an insignificant effect on the average resistance of the daisy-chained assemblies.

X-ray images of the assemblies did not reveal solder bridging, solder balling or other defects. However, the solder joints formed on PCB via-in-pad structures contained voids. The voids were present in both the solder paste and flux-assembled devices. The x-ray

Pad Type	Assembly	--------- PCB Pad Diameter ---------		
		0.011″	0.013″	0.015″
Conventional	Flux	0.0127″	0.0123″	0.0118″
Conventional	Paste	0.01325″	0.01325″	0.01325″
Via-in-Pad	Flux	0.01275″	0.0126″	0.0125″
Via-in-Pad	Paste	0.0135″	0.01375″	0.0138″

TABLE 1: Average standoff heights.

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images indicated that the voids were consistent in size (about 5% of the joint cross sectional area) and frequency (one void per joint). Thus, the void content was acceptable under the requirements of the IPC-7095 standard for BGAs. Void formation within the solder joints on the conventional PCB pads was minimal and not measured.

Cross sectioning of representative assemblies was performed to study solder joint quality, standoff height and to examine the voids observed in x-ray. Cross sectioning revealed that the solder bumps had wet well to the conventional PCB pads and resulted in excellent solder joints that showed good collapse and metallurgical bonding.

Cross sections of the solder joints formed over via-in-pad structures indicated that the numerous voids observed by x-ray were the result of gasses trapped in the via opening during the reflow process. In many instances the void remained in the via, although solder was observed along the via floor and walls.

Voids were less frequently encountered near the component attachment pad directly above the via. In these cases, the via was completely filled with solder.

In all cases, the void diameter was nearly equal to the via diameter. Cross sectional images may be found in Figure 2.

Standoff, or joint height was measured using a laser profilometer and by cross sectional analysis. Standoff is a function of package weight, I/O count, bump size, PCB pad dimensions, paste volume and other factors. The measurements strongly indicated that the standoffs of the flux-assembled devices were inversely related to the PCB pad diameters. A decrease in pad diameter results in the reduction of solderable pad area. This result, in turn, limits the amount of collapse that a solder bump may experience as it wets across the PCB pad. Thus, less collapse results in a taller solder joint.

The paste assemblies evaluated did not produce the same trend. In fact, no significant difference was observed between the standoff heights of the devices assembled to the 0.011, 0.013, and 0.015 in. diameter PCB pads. This result is due to the fact that the stencil design for this experiment

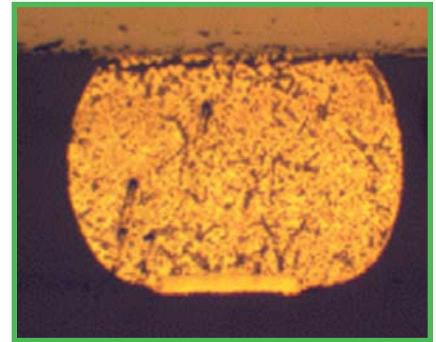

FIGURE 3: Typical fatigue failure.

incorporated larger aperture openings for the larger PCB pads. Therefore, more paste was applied on the larger pads, which compensated for the increase in solderable area. Overall, the paste assemblies produced greater standoff heights than similar flux assemblies. Standoff heights are summarized in Table 1.

Reliability Analysis

Reliability of an electronic assembly or an individual component is "the ability to function for an expected period of time without exceeding an expected acceptable failure probability." Air-to-air accelerated testing is one of the more common methods used to evaluate the reliability of electronic components. The goal is to accelerate the time-dependent wear out failure mechanism of second-level solder fatigue, which is commonly encountered in field failures.

The test used to evaluate the wafer-level assemblies was a 20-minute 0/100°C air-to-air thermal cycle consisting of five-minute dwell times at the temperature extremes and 20°C/min. transition rates between the temperature extremes.

The test specimens were monitored in-situ using a 256 channel event detection system (EDS). The EDS was programmed to record events or loop resistance measurements that exceeded 300 ohms for a minimum duration of 200 nanoseconds. Failure was defined as the cycle at which the first event was recorded that could be verified by nine additional events as described in IPC-SM-785.

Failures were frequently removed from the thermal cycle to minimize further damage to the assembly. The suspect assemblies were electrically probed to iso-

late the probable failed joint. The assembly was then cross sectioned through the suspect joint and microscopically examined.

The reliability of each sample set was calculated upon the completion of the thermal cycle test. Package reliability, or lifetime, is often reported by the number of thermal cycles required for 63.2% of a sample set to fail. The data are usually presented using two-parameter Weibull distributions that provide lifetime (N63.2) and additional information including fit, slope and N01.

Fit describes the data's deviation from a straight line. Single mechanism fatigue failures usually result in fits of 0.900 or greater. Slope, or beta values, describe the successive failure rate of the sample set. Greater slopes indicate faster fatigue rates, while a slope of less than one indicates a wear-in mechanism. N01 is the projected time (in cycles) required for 1% of the sample set to fail.

The software package used to produce the Weibull plots utilized rank regression, which generally produces conservative reliability estimates. The results of the reliability analysis were used to compare the following: conventional pad vs. via-in-pad, flux assembly vs. paste assembly and PCB pad diameter.

Results, Failure Analysis

Seventy-two packages were subjected to the thermal cycle test. The first failure occurred at cycle 309. The wafer-level package had been assembled to the 0.013 in. diameter conventional pad array with solder paste. The failure location was electrically located, but cross sectional analysis failed to determine the cause of the early failure. The second-level solder joints were continuous and showed no indication of fatigue. The next failure would not occur until cycle 1756. The second failure was identified as second-level solder fatigue (Figure 3).

The early failure had a significant impact on the reliability analysis of the wafer-level package. When included in the Weibull analysis, the predicted N01 of all the assemblies was 1,098 cycles. Exclusion from the analysis substantially increased the N01 to 1,500 cycles. However, the early failure had little impact on the N63.2 value (3,035 vs. 3,008 cycles).

Pad Type	Assembly	Pad Diameter	N01 (Cycles)	N63.2 (Cycles)	Beta	r^2
All	All	All	1500	2035	4.524	0.978
Conventional	All	All	2749	1334	6.364	0.952
Via-in-Pad	All	All	3206	1957	9.325	0.935
Conventional	Flux	0.011″	2292	3205	13.73	0.926
Conventional	Flux	0.013″	2155	2676	21.22	0.903
Conventional	Flux	0.015″	1795	2277	19.35	0.781
Conventional	Paste	0.011″	2544	3131	22.19	0.928
Conventional	Paste	0.013″	1148	2582	5.677	0.856
Conventional	Paste	0.015″	1385	2028	12.05	0.891
Via-in-Pad	Flux	0.011″	2595	3368	17.63	0.935
Via-in-Pad	Flux	0.013″	2544	3496	14.48	0.992
Via-in-Pad	Flux	0.015″	1979	2780	13.54	0.781
Via-in-Pad	Paste	0.011″	2362	3472	11.94	0.931
Via-in-Pad	Paste	0.013″	1982	3047	10.69	0.922
Via-in-Pad	Paste	0.015″	1734	2785	9.711	0.811

TABLE 2: Weibull analysis summary.

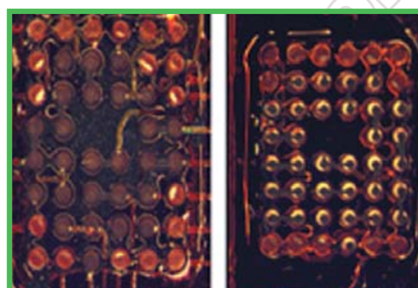

FIGURE 4: Dye penetration test results.

The Weibull reliability analysis is summarized in Table 2. Note that the early failure was excluded from the analysis because the failure mechanism was not positively identified.

Several trends are apparent from the data analysis summarized in Table 2:

- The packages assembled on via-in-pad structures produced an N63.2 16% greater than those assembled on conventional pads. Hypothesis analysis determined that the difference was significant.
- Reducing pad diameter improved solder joint reliability. Decreasing the pad diameter from 0.015 to 0.011 in. increased the N63.2 by an average of 35%. Hypothesis analysis determined that the difference was significant.
- No significant reliability difference was observed between packages assembled using solder paste and those assembled with flux with pad design constant. Flux assemblies actually produced slightly greater N63.2 values.

Cross-sectional analysis revealed that the package failure mode was predominantly solder fatigue. The fatigue failure occurred through the bulk solder material near the component attachment pad, independent of the board pad size or type. The crack formations were very fine, originating at the solder joint corners and propagating toward the solder joint center.

Electrical mapping of the failed samples showed that the solder joints containing severe fatigue were located at the outer corner of the package where the distance to neutral point (DNP) was maximum. Dye penetration tests (Figure 4) were performed, and the results supported the observations made by cross sectional and electrical analysis.

Conclusions

This experiment revealed the following conclusions:

- Wafer-level devices can be assembled in high yield using standard surface-mount practices.
- Solder joint reliability on via-in-pad features was equivalent to that on conventional pads.
- Decreasing pad diameter from 0.015 to 0.011 in. improved reliability more so than assembly with paste in place of flux.
- Joints assembled to via-in-pad structures contained a void due to gasses trapped in the via. The presence of the void did not reduce the reliability of the solder joint.

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