向无铅焊接的转换不仅要确认长期可靠性，也不仅要确认（材料组）温度剧增至从260°C发生的偏移。这种转换要确认制造可能性和测试。本论文探讨两种现成的“BGA”元件(完全一样，只是一种含铅量高，而另一种不含铅)，以便评价改变焊料的影响。如图1和图2所着重显示的，含铅量高的装置在目标负荷的情况下比无铅合金发生的变形大50%，很可能是因为铜熔化到焊料中发生合金化反应。

Pb-free Manufacturability and Test Control

Terence Q. Collier

A process for determining the sweet spot between electrical contact and mechanical deformation for lead-free solders.

A few years back, lead-free initiatives were pushed aside as a passing fad. How times have changed. Many Japanese companies have converted to lead-free, and a number of European and U.S. companies are in transition. Many design managers waited until more direction was available because they did not wish to incur the cost of redesign and requalification of product for a directive (WEEE and RoHS) with implementation dates changing as fast as the potential replacement alloy. One date for complete conversion in Japan; a different date for the European Union's deadline, coupled with resistance to change from the U.S.

Lead-free product is important for a number of reasons but two stand out. First, the semiconductor industry generates reams of waste material containing lead, material that eventually makes its way into the environment. Second, in practice operators often perform hand soldering (and generate solder fumes) in common areas away from exhaust vents. Other large-scale operations – from mining to SMT ovens – also add lead to the environment. Added to the worldwide push for environmental stewardship, it should have been apparent that the transition to lead-free was real.

Converting to lead-free is not simply verification of long-term reliability nor is it simply verification of temperature excursions (on material sets) to 260°C. Conversion to lead-free is verification of manufacturability and test. If these time-zero results cannot be met, the alloy is not a suitable replacement. If one cannot build the product and maintain control, then the process is not viable. Understanding how lead-free impacts performance and process control is central to its implementation.

When switching from lead-rich (PbR) to lead-free materials, additional variables should be added to the failure modes and effects (FMEA) process. Mechanically, lead-free materials are typically “harder” than high-lead materials. Data typically quoted in literature list the bulk properties of a solid sample (standard cubic area and mass). Unfortunately, the post-reflow solder alloy is neither in a bulk state nor is the post-reflow homogeneity consistent with the starting alloy. (Gold, copper, nickel, palladium and other metals can contaminate the alloy, changing the mechanical modulus.) Missing are convenient charts that provide mechanical deltas comparing small spheres versus bulk solids. Missing are charts that show the deltas when the target is a stud versus no-stud flip-chip die. Missing are charts that show the change in electromechanical properties of lead-free alloys.

Careful examination of the contact area between the bump and outside environment reveals that hardness has a dramatic impact on socket design, electrical contact (impedance and contact resistance) and overall yield. Not only are the lead-free alloys typically harder, the combined surface oxide/residual flux coating can have varying impact on the electrical first contact and contact resistance.

Two off-the-shelf BGA components were reviewed (same package, one PbR the other lead-free; the exact alloy composition is irrelevant for this process) to assess the impact of the solder conversion. **Figures 1** and **2** demonstrate a significant load delta to obtain similar bump deformation. (The degree of deformation directly correlates with the minimum force required on the bump to make electrical contact. The deformation selected is typical for an electrical contact using a tin-lead alloy.)

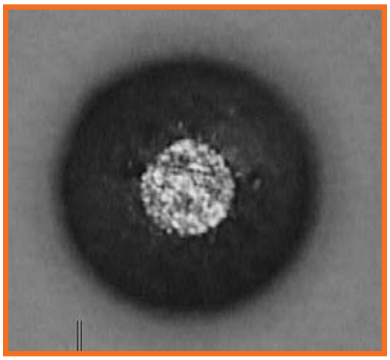

FIGURE 1: Tin-lead bump with 20 g of load. Typical contact point (flat spot) for the load.

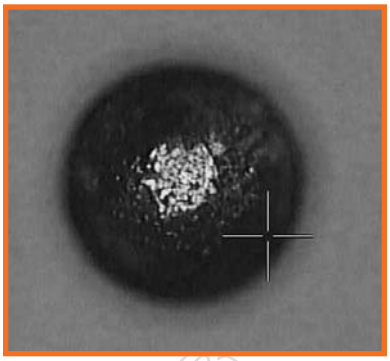

FIGURE 2: Lead-free bump with 20 g of load. Much smaller contact point on the surface.

As **Figures 3** and **4** highlight, the high-lead device will deform up to 50% more than the lead-free alloy at this target load. The high-lead device will also retain as much as 75% more deformation than the lead-free alloy after the load is removed. This phenomenon relates to the mechanical properties of the PbR solder. This phenomenon is even more pronounced on copper-studded flip-chip packages when compared to a non-stud type. Changes in the bump chemistry results in a continual change in the metallurgy and mechanics; this is likely due to dissolution and alloying of copper into the solder.

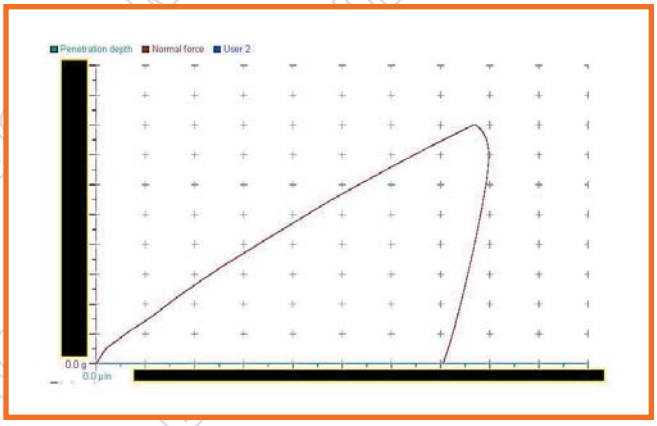

FIGURE 3: Load versus deflection curve for a tin-lead bump. The bump deforms about eight units across the scale per given load.

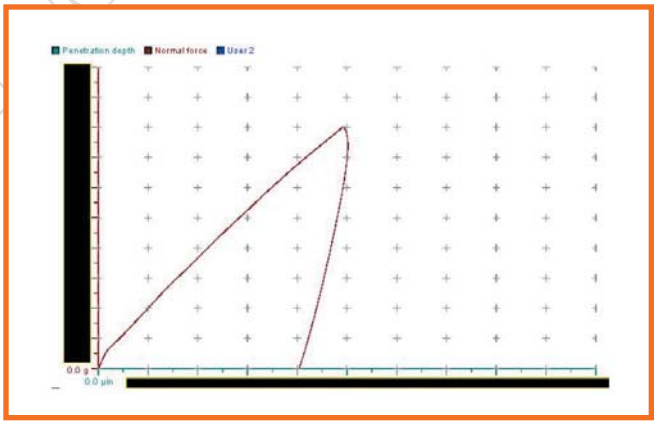

FIGURE 4: Under the same load, the lead-free bump deforms just five grids across the chart. The delta suggests possible process control issues if not properly characterized.

When looking for methods to improve BGA-to-socket or flip-chip-to-probe-card life and to understand how conversions from PbR to lead-free could impact electrical and mechanical performance, physical testing is necessary. For flip chips, to determine if yield can be improved and better process control maintained, a comparative analysis of the electromechanical properties is necessary. With the proper tool setup (this process uses a modified tool from CSM Instruments), electrical contact resistance – as well as true electrical first contact and mechanical durability – can be easily obtained.

In our evaluations, we determined the sweet spot between true electrical contact and mechanical deformation to suggest better process control. The data suggest that the conversion from PbR to lead-free is not a drop-in replacement electrically or mechanically, regardless of reflow temperature. The process also provides the investigator an early opportunity to evaluate the impact of misaligned test hardware on solder bump reliability: Slight offsets in alignment can skew results of mechanical tests on finished product.

Electromechanical data provides the process/design FMEA owner unbiased data in the alloy selection process. The ability to select the appropriate materials based on hard data versus modeling removes guesswork from engineering, resulting in "right the first time" setup, socketing and interface hardware. Electromechanical characterization for the alloy not only helps the package owner, but aids device design. Mechanically as well as electrically, silicon can be damaged due to the increased loads required to socket and test the package. Equally important, flip-chip devices with low k structures could suffer reliability issues if the force required to make electrical contact exceeds mechanical load limits.

Small geometry PbR flip chip bumps typically require between 15 to 20 grams per bump to make electrical contact.

Our team uses a modified CSM-Instruments microhardness tool to make quick estimates of the force deltas required to simulate stable electrical contact and yield. Results show lead-free material sets can require up to 70% or more load for an equivalence. (The results were validated using Kelvin connections and a four-point probe setup to show a delta of 74%. The CSM tool takes approximately 5 minutes, while the Kelvin connection can require up to two weeks to obtain results.) Instead of standard bulk resistivity and hardness, designers and process engineers should demand the type of data discussed herein from solder and sphere suppliers.

Additional variables that might rate high on the FMEA and possibly impact performance (hardware and device alike) such as flux residue, oxidation and alloy contamination should be evaluated in the same context as the bump alloy. Rinses and other processes that claim to clean bumps by removing flux residue and oxides can be added criteria to be validated in a design of experiments. The DoE process might be concluded by suggesting the correct probe needle design for the bump alloy to match prior target yields, increase throughput and optimize hardware design.

Optimizing the probe needle design to bump geometry is necessary to help prevent damage while effectively penetrating barrier layers of flux residue and oxidation to make electrical circuit (some bump deformation is required to make electrical contact; excessive load leads to damage and yield loss). This process has been streamlined from months (with marginal results) to a few days (with accurate test results). A complete analysis on solder bump deformation and electrical optimization can take less than three days with the right setups, increasing process, device and equipment optimization.

Finally, when comparing lead-free to Pb-rich solder, note that variation in durability between solder bumps on flip-chip and µBGA packages can occur due to change in scale (bump geometry of 250 µm versus 750 µm). A "deformation" delta is observed when loading at different max load values. Experimental results were in line with actual test results by less than a 5% margin of error. (Part of the error could be eliminated if the Kelvin connection had been factored.) This delta can be critical for test hardware designs, preventative maintenance (PM) and die fracture, particularly when the lead-free bump is above the low k pad. Excessive loading on a package or die could lead to hardware damage and equipment downtime. If working with lead-free solders, particularly over low-k structures, an analysis similar to the one discussed herein can be instrumental in time to market and improved reliability. ■

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