今天的数千兆赫微处理器比贴装微处理器的封装和电路板的运行速度快得多。光电子互连可能解决短距离的数据传输，但由于成本高、功率要求高、基础设施有限而且缺乏有经验的工程师而受到限制。解决这个问题的关键是设计和建立一个最佳电信号系统。本文描述一种封装和路由技术，通过封装顶部传送高频信号，通过封装底部传送低频信号。已经证明，这种技术可使用铜导线传送高达20千兆赫范围的数据。

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An Alternative PCB Architecture for High-Speed Chip-to-Chip Signal Transmission

Joseph Fjelstad

Copper's 'limits' can be stretched by routing high-speed signals through the top of the package.

Although today's optical data transmission technologies are loaded with road-blocking issues—including high cost, high power requirements, limited infrastructure and lack of experienced engineers—the need is not yet dire for the bandwidth delivery capability of fiber optics. While long-range optoelectronic signal transmission solutions are unparalleled, transmission of signals over shorter distances are more effective if the problem is approached correctly. The key to solving the problem is designing and constructing an optimal electrical signal channel. A properly designed signal channel, in copper, is capable of carrying data without pre- or post-emphasis well into the 20 GHz (40 Gbps) range.[1]

Just as the prognostications foretelling the end of Moore's Law have been destroyed by clever scientists who continue to find new ways to delay the "inevitable," so have the predictions of an early rise to optical solutions been smashed by system interconnect innovators working to extend the life of copper. Recent evidence suggests that the expected limits of signal performance with copper interconnections have also been set too low and that the performance of copper interconnections will also carry a long way into the future.

Limited expectations for copper are largely based on the historical performance of copper interconnection technology. Looking back, copper interconnection performance has moved ahead with difficulty, while semiconductor technology performance has improved in geometric fashion. However, with the proper choice of materials, PCB architecture and system design, copper interconnection technology can actually jump ahead of semiconductor technology.

The fundamental limits of copper interconnection technology are already known. Copper transmits signals at near the speed of light in air (or vacuum). Thus, if we build our circuits and suspend them in air, the limits are met. While such structures are possible in the vacuum of space, earthbound circuits must play by the laws of gravity and must somehow be supported. This support defines the basic constraint. But how does one apply the laws of physics to address the challenge? Digging a bit deeper leads to a better understanding of the problem.

In general terms, signal integrity experts view high speed in terms of signal rise time. Anything in the signal path that degrades or reduces rise time is a major impediment. In virtually every electronic design, these impediments are defined by a number of different factors. For example, the materials and interconnection path shapes that are a part of the design itself are all routinely implicated because rise time degradation is con-

tributed to by signal loss within the channel. Conductor loss, dielectric loss and impedance discontinuities manifest in a particular design (connectors, through-hole vias, material changes, manufacturing defects and the like) are primary contributors to signal degradation. With the increase in processor speeds and the speed of silicon in general, concerns once limited to the design of RF and microwave products have now been encountered by digital signal designs.

Signal Impediments

In the work of PCB design, manufacture and assembly, a number of different elements impact signal integrity at high data rates. Some common examples include inconsistencies in the physical and electrical properties of the dielectric, variations in signal trace width, changes in circuit spacing and uneven copper thickness. Even the type of foil adhesion treatment can affect the signal.[2] All of these common attributes must be taken into account as part of the signal integrity engineer's ability to accurately predict (and thus ensure maximum) performance for a given design. When tied to the range of common electrical parameters such as resistance, dielectric loss, conductor loss, stray capacitance, signal skew and inductance (which can lead to crosstalk) and the potential reflections due to electronic stubs from common circuit features such as vias, the design challenge becomes confounding.

Improvements in materials, yielding lower losses and lower dielectric constants, coupled with better manufacturing materials and processes, have yielded good performance gains. However, if one heeds what SI experts have been saying about the limiting elements of circuit design and manufacture, it is clear that there are better ways of improving the situation. One obvious solution is to simply avoid designing using traditional approaches of routing all signals within the PCB. Instead, the designer segregates and handles separately the critical signal lines on a more easily controlled signal path. This maintains the fundamental objective of high-speed circuit design to get the signal to its target as directly and cleanly as possible.

In a new package design and interconnection approach, a break from traditional methods yields the desired solution.

Knowing that the shortest distance between two points is a straight line, one can quickly envision multiple alternatives. But to achieve the objective, one must depart from traditional design layout.

ICs, using traditional interconnection approaches, have signals connecting via wire bonds or flip chip solder balls, traversing and exiting the package, traveling down through larger solder connections into the PCB and then emerging from the substrate. This path is repeated, in reverse, up through a second set of solder connections into another chip package to the chip. Clearly, the path is not optimum. Luckily, a cleaner path for signals exists. In a new package design and interconnection approach, a break from traditional methods yields the desired solution. The visual contrast (**Figure 1**) is clear and striking: High-speed signals are transmitted directly between chips with virtually no interruptions. Controlled impedance signals are launched directly off the surface of one chip package, through a controlled impedance cable, to a second package of like construction. In many applications, very simple I/O drivers requiring low power consumption are connected directly to those critical path signal lines and transmitted though the cable to the surface of the second chip package.[3,4]

'Off-the-Top' Routing

Beyond significant performance gains, the design approach has other compelling benefits. One particularly sub-

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stantial benefit is the ability to simplify both chip package design and substrate design layout, thereby reducing layer counts in both structures. Critical signals are transmitted through an "off-the-top" interconnecting medium, taking the design and manufacturing pressure off both the circuit and package, and improving overall yields. Another benefit of the technology: finished IC packages are fully tested and characterized at speed with relatively simple test fixturing (**Figure 2**). Giving credence to the concept is modeled data produced by Teraspeed Consulting Group. The model includes two packages interconnected using the prescribed OTT method at 75 mm apart and shows that signals can be transmitted easily between chips at data rates up to 25 Gbps (**Figure 3**).

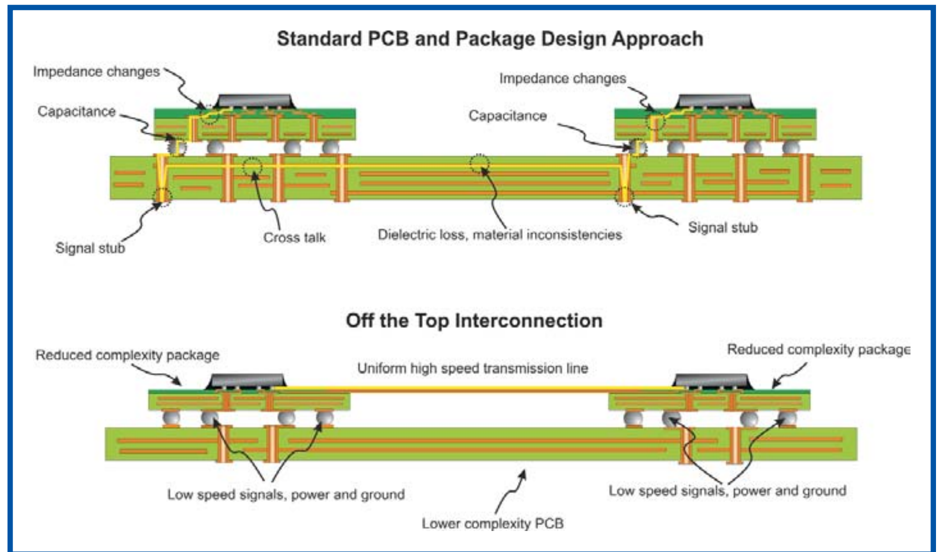


FIGURE 1: Routing high-speed signals from the top of the IC package allows the designer to avoid complex design issues and create a clean signal channel.

While the method has clear benefits, it does require changes in design tools, manufacturing and assembly. Each area is impacted, but the challenges are small and incremental. The OTT packaging, as vetted by existing IC packaging foundries, has been described as "business as usual" from an assembly perspective. Packaging foundries and select customers request strongly the ability to do full parametric testing at speed. Board-level assembly is a bit more complicated and is not presently a drop-in solution for most assemblers. However, OTT is proving a compelling option to end-users requiring high speed and low cost. Moreover, the wide application of OTT packaging technology in 10 Gbps backplanes, high-speed memory systems and FPGAs has shifted the current architectural barriers. Prototypes of the OTT package have been fabricated and measurement data are forthcoming. Ultimately, the developers believe that proposed solutions and future products based on them will meet or exceed all cost and performance design requirements with minimal disruption to the manufacturing infrastructure. ■

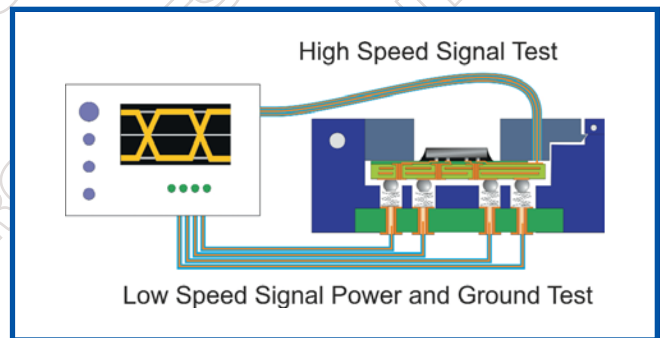
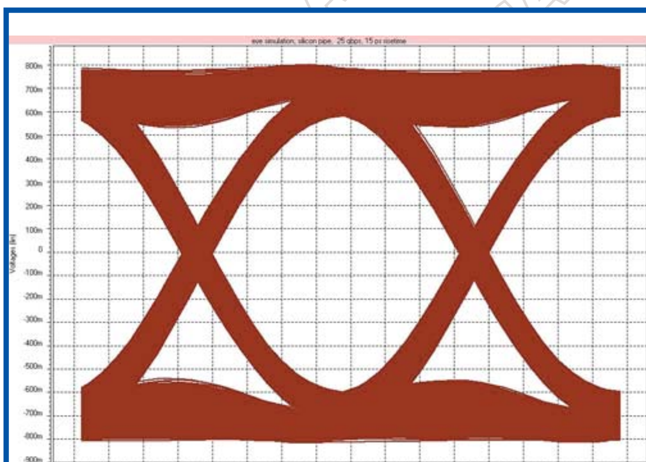


FIGURE 2: Off-the-top testing requires double-sided testing. A clamshell-type tester (illustrated) is common in board test and could be adapted to testing OTT packages.



Courtesy Teraspeed Consulting Group

FIGURE 3: Eye diagram for package-to-package interconnection with 75 mm separation between devices and including crosstalk at 25 Gbps.

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