AUSTIN, TX – Use of 3D thin silicon vias is slowing, despite a strong desire to use the technology, a new study finds.

While the drivers for 3D ICs remain constant, the timeline for adoption keeps shifting into the future, says **TechSearch International**.

In its just-released 122-page study, *3D TSV Markets: Applications, Issues, and Alternatives*, TechSearch analyzes the 3D TSV market and alternatives such as package-on-package and 2.5D (interposers with TSVs).

One major issue holding up adoption is EDA tool availability, including the ability to use thermally aware tools and the ability to communicate between tools, TechSearch found. Others include manufacturing yield in key process steps such as debonding during wafer thinning; thermal dissipation and cooling methods; test methodology; infrastructure-related issues, including logistic supply chain handoff; reliability data for a broad range of applications, and unit device cost compared to alternatives.

Once the 3D TSV technical challenges are resolved and the technology becomes cost-effective, business challenges will remain until the industry settles on a model, says TechSearch. As the boundary between foundry and assembly processes continues to blur, there will be a struggle to determine which organizations can best meet the customer's needs for assembly and test. Any one of these issues has the potential to limit a full 3D TSV implementation, and these challenges are driving many companies to seek alternative packaging and assembly solutions until they can be solved, according to the firm.

The report also contains a five-year market forecast for PoP, 2.5D, and 3D TSV applications in units and wafers.