LAS VEGAS – **iNEMI** is organizing several new efforts to help industry collaboratively address common challenges. Among the new projects scheduled for launch this spring are Pb-Free Alloy Alternatives, Pb-Free Early Failure, Boundary Scan Adoption and Solder Paste Deposition.

"iNEMI's roadmapping and gap analysis activities help us identify those technology and infrastructure gaps where it makes sense for industry to collaboratively develop common solutions," said Jim McElroy, CEO of iNEMI, in a press release. "The initiatives we are currently organizing address needs identified by the roadmaps and, in all cases, represent activities that would not have as much impact on the supply chain if undertaken by a single company."

Pb-Free Alloy Alternatives. This project is being organized to provide guidelines to help make the growing proliferation of Pb-free alloys easier to manage. Many BGA suppliers are changing the alloys used for Pb-free solder balls to improve mechanical shock performance. Suppliers are also promoting a variety of wave solder alloys to address concerns about copper dissolution, barrel fill, common wave defects, and the high cost of alloys. As a result, the variety of Pb-free alloys is increasing. Several of these alloys have lower levels of silver and, therefore, a higher melting point (up to 10°C higher), which may require a change in assembly processes. The first phase of this project will focus on the analysis of existing knowledge and assessment of critical gaps, and on driving standards to help manage supply chain complexity and risk.

Pb-Free Early Failure. This effort will determine whether a large sample size can reveal Pb-free early failures in accelerated thermal fatigue testing of Pb-free solder joints. The physical and metallurgical differences between SnPb and Pb-free solders have a direct effect on thermal cycle performance, and the properties and failure behavior of SAC solders are markedly different. If the outliers identified in Pb-free soldering thermal fatigue studies are a function of the structure/properties, they may not be visible in the relatively small sample size used in thermal cycling tests. If so, the traditional SnPb sample size (32) is inadequate to characterize the reliability of Pb-free solders, and test data using these sample sizes could result in over-estimation of reliability (i.e., small sample size could mask early Pb-free failures).

The team plans to develop a unique test vehicle with a large sample size (256 each of three different component types) to test BGA solder joints. Testing will include two components that tend to fail relatively quickly (to encourage early failure) and a third with a slightly longer life, and will cover four conditions: small sphere joints, large sphere joints, low strain rate and high strain rate.

Boundary Scan Adoption. This project will promote wider adoption of boundary scan (IEEE 1149.1, 1149.6 and P1581) throughout the industry, encourage semiconductor vendors to include the technology in their products, and promote the development of tools by ATE vendors to support boundary scan based board test.

Increasing circuit densities and speeds are quickly reducing electrical test point access for assembly test. Boundary scan is a technology that permits continued testability of assembly, but its use requires it be designed into semiconductor devices and board assemblies. Wider availability of complying devices is necessary to enable cost-efficient and effective board test for future designs. Design-for-test is currently not accepted in the general area of memory devices (SRAM, DRAM, flash, etc.). In addition, tools to support boundary scan based test need to be developed and integrated into manufacturing test equipment. This project proposes to bridge the gap between board test and board manufacturing where this lack of understanding arises in the use of design-for-test.

"We feel the standards are not being adopted, and we want to encourage more

standardization," McElroy told *Circuits Assembly*.

Solder Paste Deposition. iNEMI's first regional deployment project is currently being organized in China. The Solder Paste Deposition Project will investigate solutions to depositing different volumes of solder paste on the same board. As board density increases and components become smaller, fine-pitch components (requiring smaller volumes of solder paste) often appear next to larger components (requiring more paste), and a single-thickness stencil cannot satisfy all components in the same printing process. In these situations, a step stencil is the least expensive and most popular solution. However, the challenge is in determining the proper distance between the various components because the step stencil may affect the thickness of the solder paste deposition, especially for miniature and fine-pitch components located around the step.

The project team proposes to 1) investigate the keep-out distances of step stencils and output the design rules, 2) identify new paste deposition technologies for high-density layouts, and 3) compare and evaluate the feasibility of identified technologies, including the development of new manufacturing processes and equipment.